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Review on Extended TSPC Structures for Dynamic Logic

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I. INTRODUCTION

FROM the early days of CMOS technology up to thepresent, several clock policies have been proposed for the implementation of CMOS circuits. The number of clock phases—a major clock feature—has suffered several vicissitudes. The pseudo two-phase logic was one of the earliest techniques proposed [3]; later on, two-phase logic structures were introduced and advanced.

The domino technique [4], which prosperously associated two-phase circuits and dynamic gates, and the NORA technique [5], an extensive no race approach for two-phase and dynamic circuits, are landmarks of this advance. The first single-phase clock policy was only introduced in the tardy 1980s, called the true single-phase-clock (TSPC) [6].

Single-phase clock policies offer superior characteristics, since their utilization simplifies the clock distribution on the chip and reduces the transistor number. Thus, higher frequencies and simple designs can be achieved. In the 1990s, several incipient TSPC features were proposed [7], and among them a comprehensive extension of the TSPC [1], the elongated true-single-phase-clock CMOS circuit technique (E-TSPC); consisting of composition rules for single-phase circuits utilizing complementary static, dynamic, latch, data precharged [7], and NMOS like blocks (ratioed logic blocks) [1], [2].

This paper describes the E-TSPC circuit blocks and composition rules. It consists of four blocks such as [2]

1. Basic CMOS Blocks
2. Composition Rules
3. Exception Rule
4. NMOS-Like Logic Extension

The main purport of this paper is the exordium of incipient structures in the E-TSPC technique to build circuits handling data with rates that are twice the clock rate. These structures are composed by the connection of certain n and p data-chains, leading to lower-power consumption or higher speed (or both) circuits.

II. THE E-TSPC CIRCUIT TECHNIQUE

A. Basic CMOS Blocks

The sanctioned blocks in E-TSPC circuits have already been listed above and most of them are well-kenned blocks. Owing to the nonstandard nomenclature used and the paramountcy of the block, the latch blocks and their N-MOS like versions are shown in Fig. 1. Albeit these blocks do not execute a true latch function, their presence is indispensable in any data chain for the holding operation.

In the latch of Fig. 1, the clocked transistors of the n- and p-latches are placed proximate to the potency rail, as suggested by [8]. [2], with terms like pc or nonpc inputs, PH and PL blocks, and n-Dp and p-Dp blocks, is used in both definition 1 and Table 1.

Blocks with this configuration can attain a higher speed but suffer from charge-sharing problems. Latch configurations with clocked transistors close to the block output are also admissible. Note, that a new terminology associated with data precharged blocks [1], Data precharged blocks are blocks where the output precharges are controlled by some of the data signal inputs, the so called pc-inputs, and not by the clock signal. In a PH data precharged block, the precharge is done when all pc-inputs are high; similarly, in a PL block, the precharge is done when all pc-inputs are low. If a PH (PL) block has all of its pc-inputs high (low) whenever the clock is low, thus performing the output precharge, the block is also called a n-Dp block; likewise, if a PH (PL) block has all of its pc-inputs high (low) whenever the clock is high, the block is called a p-Dp block. In E-TSPC circuits, the block connections should be done according to composition rules. Since the concept of data-chain is fundamental for understanding the rule, the definition of data chain is presented first.

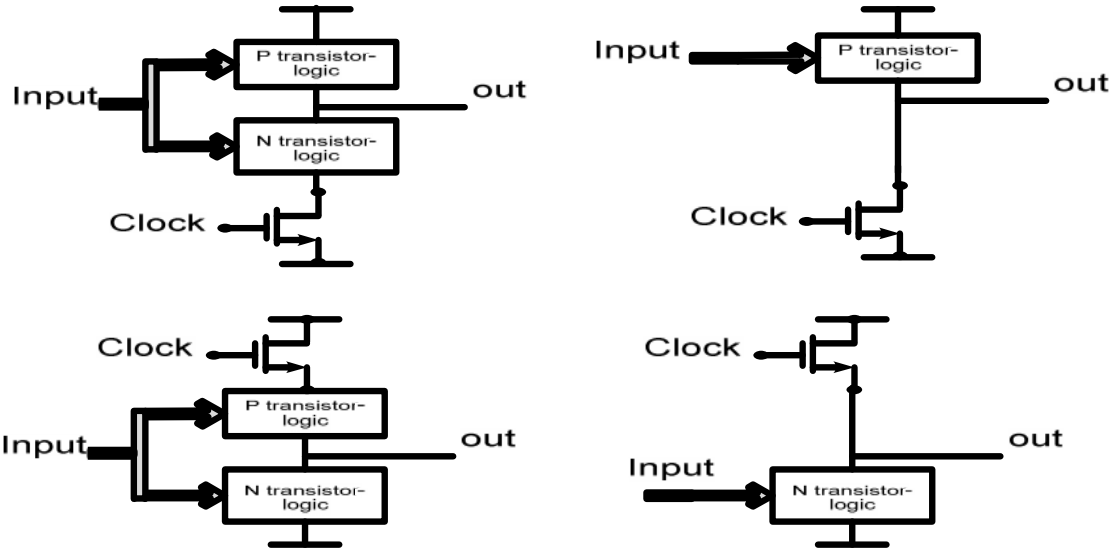

Fig. 1. The latch blocks of the E-TSPC circuit technique (a) n-latch. (b) N-MOS like n-latch. (c) P-latch (d) N-MOS like p-latch.

Table 1: Constraints between the number of inversion between adjacent block.

	Latch input	**PH block pc-input**	**PH block non-pc-input**	**PL block pc-input**	**PL block non-pc-input**	**n-dynamic input**	**p-dynamic input**
i/p of data chain	No restriction	Connection not allowed	No restriction	Connection not allowed	No restriction	No restriction	No restriction
Latch output	No restriction	Connection not allowed	Connection not allowed	Connection not allowed	Connection not allowed	Connection not allowed	Connection not allowed
PH block output	No restriction	Odd no, of block used	Odd no, of block used	Even no, of block used	Even no, of block used	Even no, of block used	Odd no, of block used
PL block output	No restriction	Even no, of block used	Even no, of block used	Odd no, of block used	Odd no, of block used	Odd no, of block used	Even no, of block used
n-dynamic output	No restriction	Even no, of block used	Even no, of block used	Odd no, of block used	Odd no, of block used	Odd no, of block used	Connection not allowed
p-dynamic output	No restriction	Odd no, of block used	Odd no, of block used	Even no, of block used	Even no, of block used	Connection not allowed	Odd no, of block used

B. Composition Rules

Definition 1: An n-data chain is any nonc yclic signal propagation path:

1) containing at least one n-latch, or one n-dynamic, or one n-Dp block;

2) starting at a circuit external input, or at the output of a p-latch, or p-dynamic, or p-Dp block; when this output is followed by static blocks in the normal data flow, the data chain starts at the output of the last static block;

3) going through static, n-dynamic, n-Dp, or n-latch blocks;

4) regardless of the number and order of the blocks defined above;
5) finishing in a circuit external output or in the input of the first p-latch, or p-dynamic, or p-Dp block. For the p-data chains, an equivalent definition applies, replacing n with p and vice-versa. When the clock is high, n-data chains are in the evaluation phase; otherwise they are in the holding phase. P data chains evaluate when the clock is low.

C. Exception Rule

In consequence, the p-latch output may change during its holding time. Consider an initial state on which the signals clock, input, and output a are low, and both blocks BL1 and BL4 are evaluating. At the end of the evaluation period, the outputs a1 and a2 are high. Subsequently, when the clock goes to high, the other blocks will evaluate. Suppose that a1 works properly, holding its former value (high). In this case, the node a2 goes to low, output a goes to high, and b1 goes to low. As a result, the transistor N1 is cut, and the final value of node b2 will depend on the circuit delays.
Commonly, the delay between nodes a1 and a2 is long enough to ensure that b2 is fully discharged through transistors N1 and N2 in this case, the second D-FF works. properly. A simple exception rule is added to cover the utilization of the well-established TSPC D-FF's Exception Rule (re): Configurations are similar where rules r4 and r5 are not obeyed, are accepted if enough delay exists. The data chains where re is applied, to the detriment of r4 and r5 do not have a latch with steady output at the holding phase.
Since the correct operation of the circuit will depend on the block delays, the exception rule should be used with caution.

D. NMOS-Like Logic Extension

When high speed is also a requirement, restrictions on the use of p-dynamic and p-latch blocks should be imposed. These Blocks have at least two p-transistors in series, which may reduce considerably the maximum speed. In such applications, the p-data chains are limited to one block, and most logic operations are handled with n-data chains with limited logic dept. Thus, deep pipelines will be necessary to implement complex and fast logic designs.
The NMOS-like blocks are faster due to the reduced number of transistors in series, but, unfortunately, they consume more power. In consequence, they should be used only in critical data chains, where the desirable speed has not been reached. Since the connection characteristics do not depend on whether it is a conventional or an NMOS-like block, the composition rules (r1-r5 and re) are valid and necessary for both; as a result, NMOS-like blocks and conventional blocks can replace one another, and the judicious selection of NMOS-like blocks is made easy.
The most challenging part of designing a prescalar is design of divider circuit as it determine speed and power consumption. Generally D flip flop is used to design the prescalar.

III. DESIGN OF D FLIP-FLOP USING TSPC & ETSPC

A. Requirements for the Flip-Flop Design

1. High speed of operation:
2. Small Clk-Output delay
3. Small setup time
4. Small hold time → Inherent race immunity
5. Low power
6. Small clock load
7. High driving capability
8. Integration of logic into flip-flop
9. Multiplexed or clock scan
10. Robustness
11. Crosstalk insensitivity

B. Sources of Noise

1. Noise on input
2. Leakage
3. α-particle and cosmic rays
4. Unrelated signal coupling
5. Power supply ripple

Sources of noise is shown in Fig. 2.

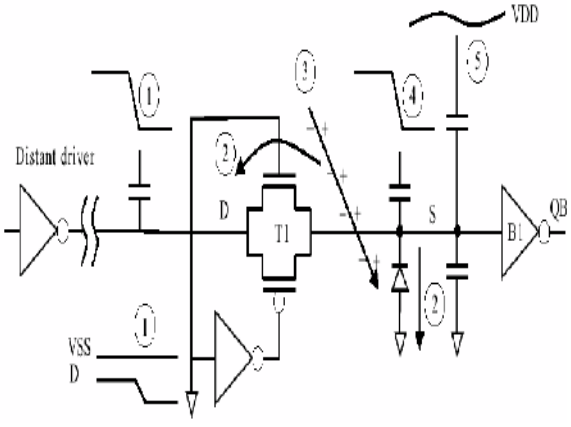

Fig. 2. Different source of noise in flip flop.

C. Flip-Flop Robustness

1. Robustness of the storage node
2. Input isolation
3. Data stored statically, max resistance limit
4. Min capacitance limit
5. Preventing storage node exposure

Dynamic flip-flops uses charge stage to store data the issue is races due to overlapping clock and the intrinsic capacitance limits the max clock frequency used. To remove this C^2MOS design of flip-flop is used the problem with C^2MOS is that when clock is in rise/fall time both NMOS&PMOS were ON causing power consumption of circuit.

So TSPCL (true single phase clock logic) is used which is actually a redesign of C^2MOS logic to use single clock, in these circuit all the transistor have to work in a single time period, no evaluation or hold period is provided to circuit as in C^2MOS logic.

Several techniques as well as sundry flip-flops have been proposed recently to reduce redundancy in clock system. There are many flip flops given in the literature [8]-[10]. Many digital and computational circuits selectively use master – slave and pulsed triggered flip-flops [6]. The paper presents diminutive area dynamic TSPCL (True Single Phase Clocked Logic) D flip-flops that were presented in [5] and [7]. These edge triggered flip-flops are minuscule in area since they exhibit low transistor count. With a simple modification, the internal\ switching at some nodes of these flip-flops is minimized in order to reduce power consumption [7].

TSPCL dynamic logic style uses just a single clock signal for synchronization and it withal reduces involution. In the design of TSPC flip-flop edge triggered (positive or negative) D flip-flop is utilized. The circuit consists of alternating stages called n-blocks and p-blocks and each block is being driven by the same clock signal. The schematic of pristine TSPC flip-flop is shown in Fig.1. In this design a single ecumenical clock signal needs to be engendered and distributed in order to simplify the design.

Fig. 3, Fig. 4 and Fig. 5, presents negative edge triggered TSPC D-flip-flop. It is operated as when the clock signal *clk* is LOW, the input is isolated from the output. When clock makes a LOW-to-HIGH the output will latch the complement of the input.

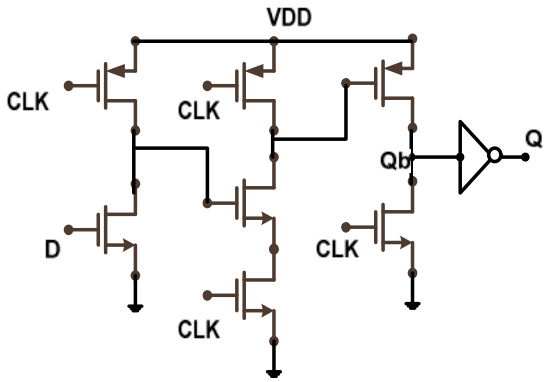

Fig. 3. D-flipflop using TSPC using 9 transistor .

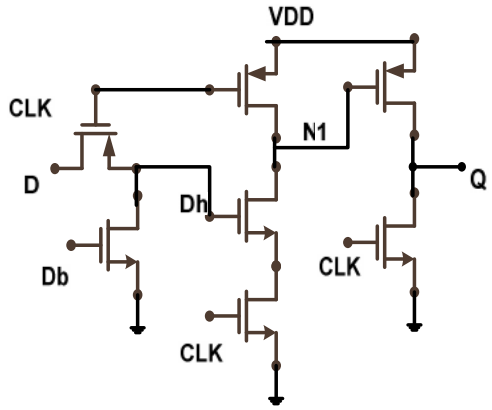

Fig. 4. D-flipflop using TSPC with using 7 transistor with folding at input to reduce transistor count.

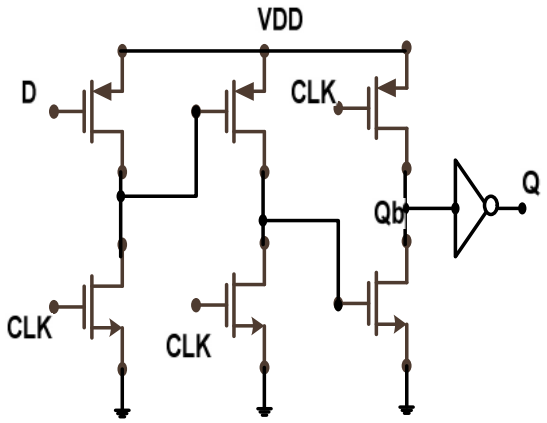

Fig. 5. D-flipflop using ETSPC with using 8 transistor.

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